SPHT: Scalable Persistent Hardware Transactions

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Abstract

With the emergence of byte-addressable Persistent Memory (PM), a number of works have recently addressed the problem of how to implement persistent transactional memory using off-the-shelf hardware transactional memory systems. In this talk I will show experimental results using Intel Optane DC PM highlighting several scalability bottlenecks that state of the art approaches incur and how our SPHT system overcomes these limitations to enhance throughput by up to 2.6× on STAMP and achieve speedups of up to 2.8× in the log replay phase.

Bio

Daniel Castro received the Master degree in Engineering Systems and Computer Engineering from Instituto Superior Técnico (University of Lisbon). He is currently a PhD student at Instituto Superior Técnico (University of Lisbon) and INESC-ID. His research interests are in transactional memory, emergent non-volatile memory, heterogeneous computing and performance systems modelling.